

Nodari Sitchinava

Curriculum Vitae

University of Hawaii at Manoa
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EDUCATION

- 2009 Ph.D. (Computer Science), *University of California, Irvine*
Thesis: “Parallel external memory model and algorithms for multicore architectures”
Advisor: Michael T. Goodrich
- 2003 M.Eng. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*
Thesis: “Dynamic scan chains – a novel architecture to lower the cost of VLSI test”
Advisors: Rohit Kapur and Daniel A. Spielman
- 2002 S.B. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*

PROFESSIONAL EXPERIENCE

- | | |
|--------------------------------------------------------------------------------------------------------|----------------------------------------------|
| University of Hawaii at Manoa
<i>Associate Professor</i> | Honolulu, HI
2019 – current |
| University of Hawaii at Manoa
<i>Assistant Professor</i> | Honolulu, HI
2014 – 2019 |
| Karlsruhe Institute of Technology
<i>Postdoctoral Researcher</i> (Host: Prof. Peter Sanders) | Karlsruhe, GERMANY
Sept. 2011 – Dec. 2013 |
| MADALGO, University of Aarhus
<i>Postdoctoral Researcher</i> (Host: Prof. Lars Arge) | Aarhus, DENMARK
Sept. 2009 – Sept. 2011 |
| Synopsys, Inc.
<i>Research & Development Engineer in VLSI Test R&D Group</i> | Mountain View, CA
Sept. 2003 – Sept. 2004 |

RESEARCH INTERESTS

Computational models for multicores and GPUs, parallel external memory and cache-oblivious algorithms, parallel data structures, energy-efficient computation, distributed processing of massive data

TEACHING EXPERIENCE

1. Lectures and Seminars

- University of Hawaii at Manoa* 2015-2020
Undergraduate course “ICS 311: Algorithms”
Taught in Spring 2020 (2), Spring 2019 (2), Spring 2018 (2), Spring 2017 (2), Fall 2015 (2), and Spring 2015
- University of Hawaii at Manoa* Fall 2019
Graduate course “ICS 621: Analysis of Algorithms”

<i>University of Hawaii at Manoa</i> Undergraduate course “ICS 491: Competitive Programming”	Fall 2018
<i>University of Hawaii at Manoa</i> Undergraduate course “ICS 443: Parallel Algorithms”	Fall 2017
<i>University of Hawaii at Manoa</i> Graduate course “ICS 643: Advanced Parallel Algorithms”	Fall 2016
<i>University of Hawaii at Manoa</i> Graduate course “ICS 691: Advanced Data Structures”	Spring 2016
<i>University of Hawaii at Manoa</i> Graduate course “ICS 691: Advanced Parallel Algorithms”	Fall 2014
<i>University of Hawaii at Manoa</i> Undergraduate course “ICS 491: Parallel Algorithms”	Spring 2014
<i>Karlsruhe Institute of Technology</i> Graduate course “Algorithms for memory hierarchies”	Winter 2012/2013
<i>Karlsruhe Institute of Technology</i> Seminar “Algorithms for realistic parallel models”	Summer 2012
<i>MADALGO, University of Aarhus</i> Graduate course “I/O-efficient graph algorithms” (together with Prof. Norbert Zeh and Dr. Deepak Ajwani)	Spring 2010
<i>MADALGO, University of Aarhus</i> Summer school on cache-oblivious algorithms (together with Professors Gerth Stølting Brodal, Erik Demaine and Norbert Zeh)	Summer 2008

2. Invited Lectures

<i>Guest Lecturer, Karlsruhe Institute of Technology</i> “Algorithms II” by Prof. Peter Sanders.	Winter 2011/2012
<i>Guest Lecturer, Karlsruhe Institute of Technology</i> “Algorithms engineering” by Prof. Peter Sanders.	Winter 2011/2012
<i>Guest Lecturer, MADALGO, Aarhus University</i> Graduate course “I/O algorithms” by Prof. Lars Arge.	Spring 2011
<i>Guest Lecturer, UC Irvine</i> Graduate course ICS 261 “Data structures” by Prof. David Eppstein.	Spring 2008

PUBLICATIONS *

1. Refereed Conference Publications

- [C-1] *K. Berney, N. Sitchinava*. Engineering worst-case inputs for pairwise Merge Sort on GPUs. In *Proceedings of the 34th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1133-1142, **2020**.

As is customary in the respective communities, the authors of the publications at the algorithmic venues are listed alphabetically, while at the high-performance computing (HPC) ones are listed in the order of contributions. The latter are marked with an asterisk (), with the main student contributor listed first and the advisor listed last. Italicized authors are Sitchinava’s students.

- [C-2] P. Afshani, R. Fagerberg, D. Hammer, R. Jacob, I. Kostitsyna, U. Meyer, M. Penschuck, N. Sitchinava. Fragile complexity of comparison-based algorithms. In *Proceedings of the 27th Annual European Symposium on Algorithms (ESA)*, pages 2:1-2:19, **2019**. **ESA Track A Best Paper Award**.
- [C-3] * B. Karsin, V. Weichert, H. Casanova, J. Iacono, N. Sitchinava. Analysis-driven engineering of comparison-based sorting algorithms on GPUs. In *Proceedings of the 32nd ACM International Conference on Supercomputing (ICS)*, pages 86-95, **2018**.
- [C-4] K. Berney, H. Casanova, A. Higuchi, B. Karsin, N. Sitchinava. Beyond binary search: parallel in-place construction of implicit search tree layouts In *Proceedings of the 32nd IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1070-1079, **2018**.
- [C-5] N. Sitchinava, D. Strash. Reconstructing generalized staircase polygons with uniform step length. In *Proceedings of the 25th International Symposium on Graph Drawing & Network Visualization (GD)*, pages 88-101, **2017**.
- [C-6] R. Jacob, N. Sitchinava. Lower bounds in the Asymmetric External Memory model. In *Proceedings of the 29th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 247-254, **2017**.
- [C-7] P. Afshani, M. deBerg, H. Casanova, B. Karsin, C. Lambrechts, N. Sitchinava, C. Tsirogiannis. An efficient algorithm for the 1D total visibility-index problem. In *Proceedings of the 19th Meeting on Algorithm Engineering & Experiments (ALENEX)*, pages 218-231, **2017**.
- [C-8] * B. Karsin, H. Casanova, N. Sitchinava. Efficient batched predecessor search in shared memory on GPUs. In *Proceedings of the IEEE International Conference on High Performance Computing (HiPC)*, **2015**.
- [C-9] P. Afshani, N. Sitchinava. Sorting and permuting without bank conflicts on GPUs. In *Proceedings of the 23rd European Symposium on Algorithms (ESA)*, pages 13-24, **2015**.
- [C-10] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. In *Proceedings of the 39th International Symposium on Mathematical Foundations of Computer Science (MFCS)*, pages 384-395, **2014**.
- [C-11] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. In *Proceedings of the 14th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT)*, pages 1-12, **2014**.
- [C-12] D. Ajwani, N. Sitchinava. Empirical evaluation of the parallel distribution sweeping framework on multicore architectures. In *Proceedings of the 21st European Symposium on Algorithms (ESA)*, pages 25-36, **2013**.
- [C-13] M. Birn, V. Osipov, P. Sanders, C. Schulz, N. Sitchinava. Efficient parallel and external matching. In *Proceedings of the 19th International Conference Euro-Par 2013 Parallel Processing (Euro-Par)*, pages 659-670, **2013**.
- [C-14] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. In *Proceedings of the 13th International Symposium on Algorithms and Data Structures (WADS)*, pages 37-48, **2013**.
- [C-15] N. Sitchinava, N. Zeh. A parallel buffer tree. In *Proceedings of the 24th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 214-223, **2012**.
- [C-16] M.T. Goodrich, N. Sitchinava, Q. Zhang. Sorting, searching and simulation in the MapReduce framework. In *Proceedings of the 22nd International Symposium on Algorithms and Computation (ISAAC)*, pages 374-383, **2011**.
- [C-17] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. In *Proceedings of the 26th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1114-1123, **2011**.

- [C-18] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. In *Proceedings of the 18th European Symposium on Algorithms (ESA)*, pages 75-86, **2010**.
- [C-19] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. In *Proceedings of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1-11, **2010**.
- [C-20] L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, **2008**.
- [C-21] D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, **2007**.
- [C-22] * N. Sitchinava, S. Samaranayake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, **2004**.
- [C-23] * S. Samaranayake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, **2003**.

2. Journal Publications

- [J-1] N. Sitchinava and D. Strash. Reconstructing generalized staircase polygons with uniform step length. *Journal of Graph Algorithms and Applications*, 22 (3): 431-459 (**2018**).
- [J-2] P. Afshani, M. deBerg, H. Casanova, B. Karsin, C. Lambrechts, N. Sitchinava, C. Tsirogiannis. An efficient algorithm for the 1D total visibility-index problem and its parallelization. *Journal of Experimental Algorithmics*, 23 (2): 2.3:1-2.3:23 (**2018**).
- [J-3] F. Meyer auf der Heide, P. Sanders, N. Sitchinava. Introduction to the special issue on SPAA 2014. *ACM Transactions on Parallel Computing*, 3 (1): 1:1-1:2 (**2016**).
- [J-4] N. Sitchinava. Computational geometry in the parallel external memory model. *SIGSPATIAL Special*, 4(2): 18-23 (**2012**).
- [J-5] * S. Samaranayake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. *IEEE Computer*, 35(10): 63-68 (**2002**).

3. Book Chapters

- [B-1] M.T. Goodrich, N. Sitchinava. Parallel algorithms in geometry. In *Handbook of Discrete and Computational Geometry*. J.E. Goodman, J. O'Rourke, C.D. Tóth (editors), 3rd edition. CRC Press, 2017.

4. Refereed Workshops (without formal proceedings)

- [W-1] N. Sitchinava, D. Strash. Reconstructing a unit-length orthogonally convex polygon from its visibility graph. *European Workshop on Computational Geometry (EuroCG)*, **2016**.
- [W-2] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2015**.
- [W-3] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2014**.

- [W-4] N. Sitchinava, V. Weichert. Provably-efficient GPU algorithms. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2013**.
- [W-5] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2013**.
- [W-6] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2011**.
- [W-7] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, **2010**.
- [W-8] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory model. *Workshop on Theory and Many-Cores (T&MC)*, **2009**.
- [W-9] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, **2004**.
- [W-10] * N. Sitchinava, S. Samaranayake, R. Kapur, F. Neveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, **2003**.
- [W-11] * N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, **2001**.

5. Patents

- [P-1] * R. Kapur, N. Sitchinava, S. Samaranayake, E. Gizdarski, F. Neveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patents 7900105, 7836368, 7836367, 7774663, 7743299, 7596733, 7418640.

INVITED PRESENTATIONS

1. Conference & Workshop Keynote Talks

- [K-1] Workshop on Scientific Computing Carpentry March 22, 2013
Title: “Data locality in high-performance computing”

2. Selected Invited Talks

- [T-1] Université Libre de Bruxelles (Host: John Iacono) June 27, 2018
Title: “Sorting in the Asymmetric External Memory Model”
- [T-2] Harvey Mudd College (Host: Ran Libeskind-Hadas) October 26, 2017
Title: “Sorting in the Asymmetric External Memory Model”
- [T-3] Technical University of Dortmund (Host: Prof. Johannes Fischer) July 28, 2017
Title: “Lower Bounds in the AEM Model”
- [T-4] IIT – Madras (Host: Prof. John Augustine) December 14, 2015
Title: “Recent algorithmic advances in GPGPU computing”
- [T-5] Algorithms Research Collaboration in Oresund Workshop (ARCO) November 27, 2015
Title: “Recent algorithmic advances in GPGPU computing”
- [T-6] University of Münster (Host: Prof. Dr. Jan Vahrenhold) August 4, 2015
Title: “Locality-conscious Parallel Algorithms for Mobile Computing”

- [T-7] 9th Scheduling for Large Systems Workshop July 1, 2014
Title: “Provably-efficient GPU algorithms”
- [T-8] University of Chile (Host: Prof. J er emy Barbay) November 27, 2013
Title: “(Dynamic) RMQ in the External Memory and Cache-oblivious models”
- [T-9] Georgetown University (Host: Prof. Jeremy T. Fineman) November 14, 2013
Title: “Locality-conscious parallel algorithms”
- [T-10] Stony Brook University (Host: Prof. Michael A. Bender) November 13, 2013
Title: “Locality-conscious parallel algorithms”
- [T-11] ETH Zurich (Host: Dr. Riko Jacob) October 14, 2013
Title: “Parallel External Memory (PEM) model and its application to GPU computing”
- [T-12] University of Kansas (Host: Prof. Joseph Evans) April 8, 2013
Title: “Data locality in high-performance computing”
- [T-13] TU Eindhoven (Host: Prof. Mark de Berg) May 4, 2012
Title: “A parallel buffer tree”
- [T-14] Georgia Institute of Technology (Host: Prof. David Bader) March 17, 2011
Title: “Parallel computing – a theoretical perspective”
- [T-15] Goethe University Frankfurt (Host: Prof. Dr. Ulrich Meyer) December 20, 2010
Title: “Parallel computing – a theoretical perspective”
- [T-16] University of California, Irvine (Host: Prof. Michael Goodrich) April 30, 2010
Title: “Geometric algorithms for private-cache chip multiprocessors”
- [T-17] Cambridge University (Host: Prof. Simon Moore) April 22, 2009
Title: “Parallel external memory model for multicore architectures”

GRANTS

- [G-1] PI, “AF: Small: Toward A Unified Model of Parallelism And Locality”, National Science Foundation (NSF Grant 1911245), **\$200,000**, 2019-2022.
- [G-2] co-PI, “Cross-Scale Spatiotemporal Modeling Using an Integrated Data Framework”, National Science Foundation (NSF Grant 1853866), **\$349,999**, 2019-2022.
- [G-3] PI, “Workshop on Parallel Algorithms and Data Structures”, National Science Foundation (NSF Grant 1930579), **\$37,094**, 2019-2020.
- [G-4] PI, “AitF: FULL: Collaborative Research: Provably Efficient GPU Algorithms”, National Science Foundation (NSF Grant 1533823), **\$416,000**, 2015-2020.
- [G-5] PI, “Hawaii Workshop on Parallel Algorithms and Data Structures”, National Science Foundation (NSF Grant 1745331), **\$40,346**, 2017-2018.

LEADERSHIP AND PROFESSIONAL SERVICE

Editorial Service

- ◇ **Guest Editor** for *ACM Transactions on Parallel Computing – Special Issue: Invited papers from SPAA 2014*

Program Committee Chairing and Organization

- ◇ **Chair & Organizer** of the *Second Hawaii Workshop on Parallel Algorithms and Data Structures*, 2019
- ◇ **Chair & Organizer** of the *First Hawaii Workshop on Parallel Algorithms and Data Structures*, 2017
- ◇ **Publicity Chair** for *ACM Symposium on Parallelism in Algorithms and Architectures*, 2015-2019
- ◇ **Chair** of the *Sixth Workshop on Massive Data Algorithmics (MASSIVE)*, 2014
- ◇ **Co-organizer** of the *24th Annual Symposium on Combinatorial Pattern Matching (CPM)*, 2013

Program Committees

- ◇ 6th International Symposium on Algorithmic Aspects of Cloud Computing (ALGO CLOUD), 2020
- ◇ 32nd ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2020
- ◇ 27th International Colloquium on Structural Information and Communication Complexity (SIROCCO), 2020
- ◇ 22nd SIAM Symposium on Algorithm Engineering & Experiments (ALENEX), 2020
- ◇ 30th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2018
- ◇ 20th Meeting on Algorithm Engineering & Experiments (ALENEX), 2018
- ◇ 31st IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2017
- ◇ 23rd IEEE International Conference on High-Performance Computing (HiPC), 2016
- ◇ 24th European Symposium on Algorithms (ESA - Track B), 2016
- ◇ 15th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT), 2016
- ◇ 30th IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2016
- ◇ Eighth Workshop on Massive Data Algorithmics (MASSIVE), 2016
- ◇ 22nd IEEE International Conference on High-Performance Computing (HiPC), 2015
- ◇ Seventh Workshop on Massive Data Algorithmics (MASSIVE), 2015
- ◇ 26th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2014
- ◇ 16th Meeting on Algorithm Engineering & Experiments (ALENEX), 2014
- ◇ Fifth Workshop on Massive Data Algorithmics (MASSIVE), 2013

Student Clubs and Activities Advising

- ◇ *Faculty Advisor*. ACM Manoa Algorithms for Competitions and Interviews (PANDA) Club
- ◇ *Faculty Advisor and Coach* for UH Manoa student teams. ACM International Collegiate Programming Contest (ICPC), 2015, 2018, 2019.

Community Outreach

- ◇ *Speaker*. Waipahu Intermediate School Career Day, Waipahu, HI, 2014-2016, 2018-2020
- ◇ *Speaker*. Leilehua High School Career Day, Wahiawa, HI, 2014, 2019