

# Nodari Sitchinava

## Curriculum Vitae

University of Hawaii, Manoa

Department of Information and Computer Sciences

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## Education

- 2009 Ph.D. (Computer Science), *University of California, Irvine*  
Thesis: “Parallel external memory model and algorithms for multicore architectures”  
Advisor: Michael T. Goodrich
- 2003 M.Eng. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*  
Thesis: “Dynamic scan chains – a novel architecture to lower the cost of VLSI test”  
Advisors: Rohit Kapur and Daniel A. Spielman
- 2002 S.B. (Electrical Engineering and Computer Science), *Massachusetts Inst. of Technology*

## Professional Experience

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| <b>University of Hawaii, Manoa</b><br><i>Assistant Professor</i>                                       | Honolulu, HI<br>Jan. 2014 – present          |
| <b>Karlsruhe Institute of Technology</b><br><i>Postdoctoral Researcher</i> (Host: Prof. Peter Sanders) | Karlsruhe, GERMANY<br>Sept. 2011 – Dec. 2013 |
| <b>MADALGO, University of Aarhus</b><br><i>Postdoctoral Researcher</i> (Host: Prof. Lars Arge)         | Aarhus, DENMARK<br>Sept. 2009 – Sept. 2011   |
| <b>Synopsys, Inc.</b><br><i>Research &amp; Development Engineer in VLSI Test R&amp;D Group</i>         | Mountain View, CA<br>Sept. 2003 – Sept. 2004 |

## Research Interests

Computational models for multicores and GPUs, parallel external memory and cache-oblivious algorithms, parallel data structures, energy-efficient computation, distributed processing of massive data

## Teaching Experience

### 1. Lectures and Seminars

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| <i>University of Hawaii at Manoa</i><br>Undergraduate course “ICS 443: Parallel Algorithms”      | Fall 2017   |
| <i>University of Hawaii at Manoa</i><br>Undergraduate course “ICS 311: Algorithms”, two sections | Spring 2017 |
| <i>University of Hawaii at Manoa</i><br>Graduate course “ICS 643: Advanced Parallel Algorithms”  | Fall 2016   |
| <i>University of Hawaii at Manoa</i><br>Graduate course “ICS 691: Advanced Data Structures”      | Spring 2016 |
| <i>University of Hawaii at Manoa</i><br>Undergraduate course “ICS 311: Algorithms”, two sections | Fall 2015   |

<i>University of Hawaii at Manoa</i> Undergraduate course “ICS 311: Algorithms”	Spring 2015
<i>University of Hawaii at Manoa</i> Graduate course “ICS 691: Advanced Parallel Algorithms”	Fall 2014
<i>University of Hawaii at Manoa</i> Undergraduate course “ICS 491: Parallel Algorithms”	Spring 2014
<i>Karlsruhe Institute of Technology</i> Graduate course “Algorithms for memory hierarchies”	Winter 2012/2013
<i>Karlsruhe Institute of Technology</i> Seminar “Algorithms for realistic parallel models”	Summer 2012
<i>MADALGO, University of Aarhus</i> Graduate course “I/O-efficient graph algorithms” (together with Prof. Norbert Zeh and Dr. Deepak Ajwani)	Spring 2010
<i>MADALGO, University of Aarhus</i> Summer school on cache-oblivious algorithms (together with Professors Gerth Stølting Brodal, Erik Demaine and Norbert Zeh)	Summer 2008

## 2. Invited Lectures

<i>Guest Lecturer, Karlsruhe Institute of Technology</i> “Algorithms II” by Prof. Peter Sanders.	Winter 2011/2012
<i>Guest Lecturer, Karlsruhe Institute of Technology</i> “Algorithms engineering” by Prof. Peter Sanders.	Winter 2011/2012
<i>Guest Lecturer, MADALGO, Aarhus University</i> Graduate course “I/O algorithms” by Prof. Lars Arge.	Spring 2011
<i>Guest Lecturer, UC Irvine</i> Graduate course ICS 261 “Data structures” by Prof. David Eppstein.	Spring 2008

Publications (alphabetical author order, except when marked with \*)

## 1. Refereed Conference Publications

- [C-1] N. Sitchinava, D. Strash. Reconstructing generalized staircase polygons with uniform step length. In *Proceedings of the 25th International Symposium on Graph Drawing & Network Visualization (GD)*, 2017. To appear.
- [C-2] R. Jacob, N. Sitchinava. Lower bounds in the Asymmetric External Memory model. In *Proceedings of the 29th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 247-254, 2017.
- [C-3] P. Afshani, M. deBerg, H. Casanova, B. Karsin, C. Lambrechts, N. Sitchinava, C. Tsirogiannis. An efficient algorithm for the 1D total visibility-index problem. In *Proceedings of the 19th Meeting on Algorithm Engineering & Experiments (ALENEX)*, pages 218-231, 2017.
- [C-4] \* B. Karsin, H. Casanova, N. Sitchinava. Efficient batched predecessor search in shared memory on GPUs. In *Proceedings of the IEEE International Conference on High Performance Computing (HiPC)*, 2015.
- [C-5] P. Afshani, N. Sitchinava. Sorting and permuting without bank conflicts on GPUs. In *Proceedings of the 23rd European Symposium on Algorithms (ESA)*, pages 13-24, 2015.
- [C-6] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. In *Proceedings of the 39th International Symposium on Mathematical Foundations of Computer Science (MFCS)*, pages 384-395, 2014.

- [C-7] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. In *Proceedings of the 14th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT)*, pages 1-12, 2014.
- [C-8] D. Ajwani, N. Sitchinava. Empirical evaluation of the parallel distribution sweeping framework on multicore architectures. In *Proceedings of the 21st European Symposium on Algorithms (ESA)*, pages 25-36, 2013.
- [C-9] M. Birn, V. Osipov, P. Sanders, C. Schulz, N. Sitchinava. Efficient parallel and external matching. In *Proceedings of the 19th International Conference Euro-Par 2013 Parallel Processing (Euro-Par)*, pages 659-670, 2013.
- [C-10] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. In *Proceedings of the 13th International Symposium on Algorithms and Data Structures (WADS)*, pages 37-48, 2013.
- [C-11] N. Sitchinava, N. Zeh. A parallel buffer tree. In *Proceedings of the 24th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 214-223, 2012.
- [C-12] M.T. Goodrich, N. Sitchinava, Q. Zhang. Sorting, searching and simulation in the MapReduce framework. In *Proceedings of the 22nd International Symposium on Algorithms and Computation (ISAAC)*, pages 374-383, 2011.
- [C-13] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. In *Proceedings of the 26th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1114-1123, 2011.
- [C-14] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. In *Proceedings of the 18th European Symposium on Algorithms (ESA)*, pages 75-86, 2010.
- [C-15] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory graph algorithms. In *Proceedings of the 25th IEEE International Parallel & Distributed Processing Symposium (IPDPS)*, pages 1-11, 2010.
- [C-16] L. Arge, M.T. Goodrich, M. Nelson, N. Sitchinava. Fundamental parallel algorithms for private-cache chip multiprocessors. In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)*, pages 197-206, 2008.
- [C-17] D. Eppstein, M.T. Goodrich, N. Sitchinava. Guard placement for efficient point-in-polygon proofs. In *Proceedings of the 23rd Annual ACM Symposium on Computational Geometry (SoCG)*, pages 27-36, 2007.
- [C-18] \* N. Sitchinava, S. Samaranyake, R. Kapur, E. Gizdarski, F. Neuveux, T.W. Williams. Changing scan enable during shift. In *Proceedings of the 22nd IEEE VLSI Test Symposium (VTS)*, pages 73-78, 2004.
- [C-19] \* S. Samaranyake, E. Gizdarski, N. Sitchinava, F. Neuveux, R. Kapur, T.W. Williams. A reconfigurable shared scan-in architecture. In *Proceedings of the 21st IEEE VLSI Test Symposium (VTS)*, pages 9-14, 2003.

## 2. Journal Publications

- [J-1] N. Sitchinava. Computational geometry in the parallel external memory model. *SIGSPATIAL Special 4(2)*: 18-23 (2012).
- [J-2] \* S. Samaranyake, N. Sitchinava, R. Kapur, M. Amin, T.W. Williams. Dynamic Scan: driving down the cost of test. *IEEE Computer 35(10)*: 63-68 (2002).

## 3. Patents

- [P-1] \* R. Kapur, N. Sitchinava, S. Samaranyake, E. Gizdarski, F. Neuveux, S. Duggirala, T.W. Williams. Dynamically reconfigurable shared scan-in test architecture. US Patents 7900105, 7836368, 7836367, 7774663, 7743299, 7596733, 7418640.

#### 4. Refereed Workshop Presentations

- [W-1] N. Sitchinava, D. Strash. Reconstructing a unit-length orthogonally convex polygon from its visibility graph. *European Workshop on Computational Geometry (EuroCG)*, 2016.
- [W-2] R. Jacob, T. Lieber, N. Sitchinava. On the complexity of list ranking in the parallel external memory model. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2015.
- [W-3] P. Afshani, N. Sitchinava. I/O-efficient range minima queries. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2014.
- [W-4] N. Sitchinava, V. Weichert. Provably-efficient GPU algorithms. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2013.
- [W-5] L. Arge, J. Fischer, P. Sanders, N. Sitchinava. On (dynamic) range minimum queries in external memory. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2013.
- [W-6] D. Ajwani, N. Sitchinava, N. Zeh. I/O-optimal distribution sweeping on private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2011.
- [W-7] D. Ajwani, N. Sitchinava, N. Zeh. Geometric algorithms for private-cache chip multiprocessors. *Workshop on Massive Data Algorithmics (MASSIVE)*, 2010.
- [W-8] L. Arge, M.T. Goodrich, N. Sitchinava. Parallel external memory model. *Workshop on Theory and Many-Cores (T&MC)*, 2009.
- [W-9] \* N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams. Dynamically reconfigurable shared scan-in architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2004.
- [W-10] \* N. Sitchinava, S. Samaranayake, R. Kapur, F. Neuveux, E. Gizdarski, T.W. Williams, D. Spielman. A segment identification algorithms for a dynamic scan architecture. *IEEE International Test Synthesis Workshop (ITSW)*, 2003.
- [W-11] \* N. Sitchinava, S. Samaranayake, R. Kapur, M. Amin, T.W. Williams. DFT – ATE solution to lower the cost of test. *IEEE Workshop on Test Resource Partitioning*, 2001.

#### Conference and Workshop Keynote Talks

“Data locality in high-performance computing”, Workshop on Scientific Computing Carpentry, 2013

#### Selected Invited Talks

Technical University of Dortmund, (Host: Prof. Johannes Fischer) Title: “Lower Bounds in the AEM Model”	July 28, 2017
IIT – Madras (Host: Prof. John Augustine) Title: “Recent algorithmic advances in GPGPU computing”	December 14, 2015
Algorithms Research Collaboration in Oresund Workshop (ARCO) Title: “Recent algorithmic advances in GPGPU computing”	November 27, 2015
University of Münster (Host: Prof. Dr. Jan Vahrenhold) Title: “Locality-conscious Parallel Algorithms for Mobile Computing”	August 4, 2015
9th Scheduling for Large Systems Workshop Title: “Provably-efficient GPU algorithms”	July 1, 2014
University of Chile (Host: Prof. Jérémy Barbay) Title: “(Dynamic) RMQ in the External Memory and Cache-oblivious models”	November 27, 2013
Georgetown University (Host: Prof. Jeremy T. Fineman) Title: “Locality-conscious parallel algorithms”	November 14, 2013

Stony Brook University (Host: Prof. Michael A. Bender) Title: “Locality-conscious parallel algorithms”	November 13, 2013
University of Patras (Host: Prof. Christos D. Zaroliagis) Title: “PEM model and its application to GPU computing”	October 22, 2013
University of Ljubljana (Host: Prof. Andrej Brodnik) Title: “Locality-conscious parallel algorithms”	October 17, 2013
ETH Zurich (Host: Dr. Riko Jacob) Title: “Parallel External Memory (PEM) model and its application to GPU computing”	October 14, 2013
University of Kansas (Host: Prof. Joseph Evans) Title: “Data locality in high-performance computing”	April 8, 2013
TU Eindhoven (Host: Prof. Mark de Berg) Title: “A parallel buffer tree”	May 4, 2012
Georgia Institute of Technology (Host: Prof. David Bader) Title: “Parallel computing – a theoretical perspective”	March 17, 2011
Goethe University Frankfurt (Host: Prof. Dr. Ulrich Meyer) Title: “Parallel computing – a theoretical perspective”	December 20, 2010
University of California, Irvine (Host: Prof. Michael Goodrich) Title: “Geometric algorithms for private-cache chip multiprocessors”	April 30, 2010
Cambridge University (Host: Prof. Simon Moore) Title: “Parallel external memory model for multicore architectures”	April 22, 2009
Dalhousie University (Host: Prof. Norbert Zeh) Title: “Parallel external memory model for multicore architectures”	October 16, 2008

## Leadership and Professional Service

### *Program Committee Service:*

- ◇ 20th Meeting on Algorithm Engineering & Experiments (ALENEX), 2018
- ◇ 31st IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2017
- ◇ 23rd IEEE International Conference on High-Performance Computing (HiPC), 2016
- ◇ 24th European Symposium on Algorithms (ESA - Track B), Aarhus, Denmark, 2016
- ◇ 15th Scandinavian Symposium and Workshops on Algorithm Theory (SWAT), 2016
- ◇ 30th IEEE International Parallel & Distributed Processing Symposium (IPDPS), 2016
- ◇ Eighth Workshop on Massive Data Algorithmics (MASSIVE), 2016
- ◇ 22nd IEEE International Conference on High-Performance Computing (HiPC), 2015
- ◇ Seventh Workshop on Massive Data Algorithmics (MASSIVE), 2015
- ◇ *Chair*, Sixth Workshop on Massive Data Algorithmics (MASSIVE), 2014
- ◇ 26th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA), 2014
- ◇ 16th Meeting on Algorithm Engineering & Experiments (ALENEX), 2014
- ◇ Fifth Workshop on Massive Data Algorithmics (MASSIVE), 2013

### *Guest Editor:*

- ◇ ACM Transactions on Parallel Computing – Special Issue: Invited papers from SPAA 2014

### *External Reviewer (Journals):*

- ◇ Journal of the ACM (JACM)
- ◇ Algorithmica

- ◇ ACM Transactions on Parallel Computing
- ◇ Theoretical Computer Science
- ◇ Journal of Discrete Algorithms (JDA)
- ◇ International Journal of Computational Geometry and Applications (IJCGA)
- ◇ IEEE Transactions on Parallel and Distributed Systems (TPDS)
- ◇ Parallel Computing
- ◇ Computational Geometry: Theory and Applications (CGTA)
- ◇ ACM Transactions on Spatial Algorithms and Systems (TSAS)

*External Reviewer (Conferences):*

- ◇ ACM-SIAM Symposium on Discrete Algorithms (SODA)
- ◇ International Colloquium on Automata, Languages, and Programming (ICALP)
- ◇ Europeans Symposium on Algorithms (ESA)
- ◇ ACM Symposium on Parallelism in Algorithms and Architectures (SPAA)
- ◇ IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- ◇ International Symposium on Algorithms and Computation (ISAAC)
- ◇ ACM SIGSPATIAL International Conference on Advances in Geographic Information Systems (ACM SIGSPATIAL GIS)
- ◇ Symposium on Experimental Algorithms (SEA)
- ◇ Latin American Theoretical Informatics Symposium (LATIN)
- ◇ International Conference Euro-Par Parallel Processing (Euro-Par)

## Grants

1. PI, “AitF: FULL: Collaborative Research: Provably Efficient GPU Algorithms”, National Science Foundation (NSF Grant 1533823), \$400,000, 2015-2019.
2. PI, “Hawaiian Workshop on Parallel Algorithms and Data Structures”, National Science Foundation (NSF Grant 1745331), \$40,346, 2017-2018.